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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,305	07/02/2003	Christian N. Mohr	501334.01	4308

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2178	

DATE MAILED: 06/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/613,305	MOHR ET AL.
	Examiner	Art Unit
	Dang T Nguyen	2178

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 14-50* is/are allowed.

6)☒ Claim(s) *8-11 and 51* is/are rejected.

7)☒ Claim(s) *12,13 and 52-54* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 July 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on July 2, 2003.

2. Claims 1 - 54 are pending in this case. Claims 1, 8, 14, 20, 27, 33, 40, 46, and 51 are independent claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 8 - 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagai et al., U.s. Patent No. 6,434,064 B2 – filed Jun. 26, 2001.

Regarding independent claim 8, Figs. 1 and 2 of Naigai disclose a redundancy address decoder (SRD, SCD) for a memory device having a memory array divided into at least one bank of memory (Fig. 1), each bank of memory segmented into a plurality of memory blocks having a respective redundancy plane of redundant memory (Fig. 1 [16 spare word line: Col. 9 lines 54 – 65]; Fig. 2 [2 SCSL: Col. 10 lines 18 – 27]), the redundancy address decoder (Fig. 1[SRD], Fig. 2[SCD]) comprising:

for each redundancy plane in the bank of memory (Fig. 1[16 Spare word line], Fig. 2 [2 spare SCSL]), a programmable element block (Fig. 3 [Fuse Units]), redundancy comparison logic (Fig. 3 [CMP]) coupled to the programmable element block, and a redundancy driver (Fig. 3 [32]) coupled to the redundancy comparison logic, the redundancy driver having input address terminals (Fig. 3 [rA0 – cB2]) at which memory address signals (Fig. 3 [rA0 – cB2]) corresponding to a memory address are applied (Fig. 3 [row bank address, Column bank address]) and having output address terminals (Fig. 3 [A0 – B2]) to which the memory address signals are coupled in response to activation of the redundancy driver (Fig. 3 [Row-not-Col signal to input terminal of Sel 32]), the comparison logic (Fig. 3[Comparator]) comparing the memory address signals (Fig. 3 [A0 – B2]) from the redundancy driver (Fig.1 [32]) to redundancy memory addresses stored in the programmable element block (Fig. 3 [Fuse Unit]) and generating a match signal (Fig. 3 [Match output signal from 31]) in response to detecting an address match between the memory address signals and a redundancy memory address; and

redundancy driver select logic (Fig.3 [Fuse Unit f12; row/column select Fuse]) coupled to each redundancy driver (Fig. 3 [32]) of the bank of memory, the redundancy driver (Fig. 3[32]) selecting a redundancy driver (Fig. 3 [rA0 or cA0, -------, rB2 or cB2]) to activate (Row or Column) in response to receiving a selection signal (Fig. 3 [row-not-column input signal of 32]) indicative of the memory block (Row or Column of A0 – B2) in which a memory location corresponding to the memory address is located (Fig. 3 [A0 – B2]).

Regarding dependent claim 9, the redundancy driver of Fig. 3 [32] of Nagai discloses wherein the redundancy driver comprises logic circuitry (Fig. 8) to block the switching (Fig. 8[TG]) of the logic states (Fig. 8[Row-not Col]) of the memory address signals applied to the respective redundancy comparison logic when deactivated, and to allow the switching (Fig. 8[TG]) of logic states (Row or Col.) of the memory address signals applied to the respective redundancy comparison logic when activated (Fig. 8).

Regarding dependent claim 10, Fig. 3 of Nagai further discloses wherein the programmable element block (Fig. 3 [Fuse Unit]) comprises a plurality of antifuse elements programmed with column addresses of memory locations mapped to the respective redundancy plane.

Regarding dependent claim 11, Fig. 3 of Nagai discloses wherein the selection signals (Fig. 3[row-not-col]) comprise a portion of a row address (Fig. 3 [rA0 – rB2]).

Claims 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Ladner et al., U.s. Patent No. 6,552,937 B2 – filed Mar. 28, 2001.

Regarding independent claim 51, Fig. 5 of Ladner et al. discloses a method of determining mapping of memory locations (ROW ADD 3, ROW ADD 2) corresponding to row and column memory addresses in a bank (Row 0 – Row 15) of memory segment into memory blocks (COLUMN SEGMENT 0 – COLUMN SEGMENT 3) having a respective redundancy plane (Fig. 2 [REDUNDANCY COLUMN SELECT]) and antifuse block (Fig. 2 [201]), the antifuse block storing programmed address of memory locations (Fig. 2 [220 a', 220a", 220 a"', 220 a"") in the respective memory block mapped to the

respective redundancy plane (Fig. 2 [217]), the method comprising: evaluating a portion of the row memory address (Fig. 5 [11, 10, 01, 00]) to identify in which of the memory blocks the memory location is located (COLUMN SEGMENT 0 - 3); and comparing the column address to the programmed addresses (Fig. 6 [217]) of only the antifuse block of the redundancy plane for the memory block in which the memory location is located (Col. 3 lines 47 – 65).

Allowable Subject Matter

4. Claims 12 – 13, and 52 – 54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: With regard to claim 12, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "the redundancy driver select logic comprises a plurality of NOR gates, each NOR gate having a different combination of the selection signal and its complement as input signals".

With regard to claim 13, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "the redundancy driver comprises a plurality of NAND gates, each NAND gate having a first input coupled to the redundancy driver select logic and a second input to a respective of the input address terminals".

With regard to claim 52, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "blocking the column address signals

from comparison with the programmed addresses of the programmable element blocks for the remaining redundancy planes"

5. Claims 1-7 and 14 – 50 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: With regard to claims 1, 20, and 33, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "redundancy driver select logic coupled to each of the redundancy comparison circuitry to activate a selected one of the redundancy comparison circuitry for comparing a portion of a memory address corresponding to a memory location with the programmed addresses of the respective programmable element blocks, the activation by the redundancy driver based on the memory block in which the memory location is located".

With regard to claim 14, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "redundancy comparison selection circuit coupled to each of the redundancy comparison circuitry and having a control signal terminal to which at least one row address signal is applied, the redundancy comparison selection circuit generating an activation signal for activating one of the redundancy comparison circuitry in accordance with the row address signal".

With regard to claims 27 and 40, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "redundancy driver select logic coupled to each redundancy driver of the bank of memory the redundancy driver selecting a redundancy driver to activate in response to receiving a selection signal

indicative of the memory block in which a memory location corresponding to the memory address is located".

With regard to claim 46, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest " blocking the memory address from comparison with the programmed addresses of the programmable element blocks for non-selected redundancy planes".

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ooishi	Patent No. US 6,519,192 B2	Date of Patent: Feb. 11, 2003
Keeth	Patent No. US 6,314,030 B1	Date of Patent: Nov. 6, 2001
Menke et al.	Patent No. US 6,466,493 B1	Date of Patent: Oct. 15, 2002
Manning et al.	Patent No. US 6,301,164 B1	Date of Patent: Oct. 9, 2001

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (703) 305-1673. Normal contact times are M-F, 8-4:30.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Heather Herndon, may be reached at (703) 308-5186.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239 (for formal communications intended for entry)

or:

(703) 746-7238 (for after-final communications)

Hand-delivered responses should be brought to

Crystal Park II, 2121 Crystal Drive

Arlington, VA, Fourth Floor (receptionist).

Dang Nguyen 5/24/2004

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800